Impact of CSP Assembly Underfill on Reliability

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ABSTRACT

This paper reviews the package trend towards miniature scale package (CSP). The industry definition of CSP has evolved as technology and infrastructure for finer pitch become more readily available. To keep up with such definition, CSPs are considered to be miniature new packages that industry is starting to implement, and there are many unresolved technical issues associated with their implementation. One key issue yet to be fully addressed is the CSP interconnection reliability and effects of manufacturing variables. Understanding quality and assembly reliability issues associated with implementation of CSPs were the main objectives of the JPL-led CSP Consortium with representative from government agencies and private companies. Our experience gained in the process of build of 150 test vehicles with eleven CSPs in the areas of technology implementation challenges, including design and building both standard and microvia boards, and assembly of two types of test vehicles are presented. Several assemblies were underfilled to determine the effects of underfill on the level of reliability improvements. Thermal cycling test results under four environmental conditions for assemblies with and without underfills were also presented.

CSP Definition

Although the expression "CSP" is widely used by industry both suppliers and users, its definition had evolved as the technology has matured. At the start of the package's introduction into the market, a very precise definition was adopted by a group of industry experts. CSP was defined as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Soon, it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package.

A rapid transition to a much lower size was difficult both for package suppliers and end users. Suppliers had difficulty in building such packages whereas the users had difficulties in accommodating the need for the new microvia printed circuit board (PWB), chiefly, because of routing requirements and its increased cost. Other issues for accepting the "interim definition" by industry included needed maturity in assembly and infrastructure. For example, the use of pitches other than 0.5 mm, including 0.75 and 0.65, was aimed at using a standard PWB design rather than a microvia build to avoid the elevated cost of the latter.

The "expert definition" undermines one of the key purpose of the packages allowing for die shrinkage. If die shrinkage is acceptable for the package to retain the footprint, then a decrease in die size for the same CSP will change the term CSP for that package.

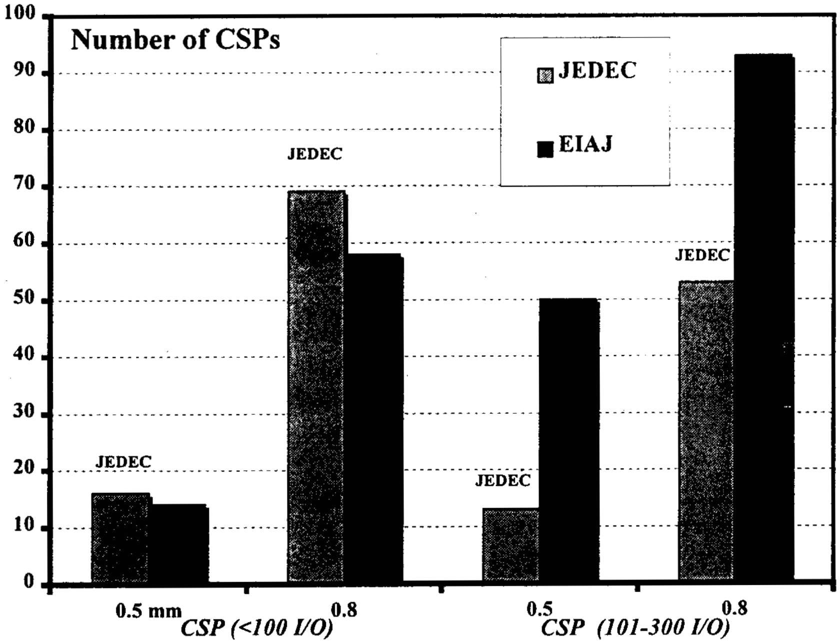
Therefore, in reality, CSPs are miniature new packages that industry is starting to implement, and there are many unresolved technical issues associated with their implementation. Technical issues themselves also change as packages mature. For example, in early 1997, packages with 1 mm pitch and lower were the dominant CSPs, whereas in early 1998 packages with 0.8 mm and lower became the norm for CSPs. New issues included the use of flip chip die rather than wire bond die in the CSP. Flip chip failure within the package is a potential new failure mechanism that needs to be considered.

JEDEC Survey on CSP

Figure 1 shows the results of surveys from JEDEC (US) and EIAJ (Japan) team members generated from data in reference 1. Surveys were carried out in 1998 regarding the status of activity in development and production of grid CSPs. For CSPs with low I/Os (<100), both US (JEDEC) and Japan (EIAJ) have approximately similar activities. This is not true for CSPs with I/Os above 100. For higher I/O ranges (100-300), EIAJ activities become two to three times more than JEDEC's. One JEDEC member reported the development of a package with 0.4 mm pitch in 500 I/O range.

The JPL-CSP Consortium experience on the availability of daisy chain CSPs for characterization of assembly reliability followed a similar trend on package I/O and pitch. CSP availability and delivery on time was one of the most challenging issue. For example, at the start of the program, in early 1997, I/Os ranged from 12 to 540 to meet the short and longer term applications. The 540 I/O/ 0.5 mm package was dropped by the manufacturer prior to the trial test vehicle assembly. Three other higher I/O with 0.5 mm pitch were not delivered. Two of these were not delivered due to package interposer issues. Another one, was a hard metric, 0.5 mm CSP package with 188 I/Os, in which its reliability data was given by the supplier for its English pitch version. The supplier was unable to meet even our last build scheduled in late 1998.

Late and lack of delivery clearly indicate that the package suppliers were struggling to build CSPs with 0.5 mm pitch, especially with high I/O counts. The majority of the follow on program, started in early 1998, have pitches of 0.8 mm similar to the JEDEC findings . In this phase, there are a few high I/O CSPs with 0.5 mm pitch. This clearly indicates that industry is starting to be more comfortable with moving towards a tighter pitch at higher I/O as also was found by the survey.



CSP Pitch and I/O Range Categories

Figure 1 Survey of Package I/O and Pitch for US and Japan Industries

CSP RELIABILITY

CSPs have their own unique form factor not seen in SMT and many of them may not be able to meet the traditional reliability test requirements. There is a paradigm shift on reliability for CSP and new specific tests such as bend and drop tests are being adopted to especially meet consumer portable requirements. The shift is further motivated by several factors including the following:

- Reduction in life expectancy for consumer electronics
- Rapid changes in electronic technology

For surface mount, solder has both electrical and mechanical functions and has been the weakest link in assembly reliability. This means that damage to solder could readily affect functional integrity of the microelectronics system. Therefore, defects that cause changes either in mechanical or electrical system characteristics and understanding their reasons for failure are critical. The most common damage to solder joints are those induced by thermal cycling. Creep and stress relaxation are main causes of cycling damage. Creep for materials generally occurs at temperatures above half of the absolute melting temperature ($T/T_m > 0.5$). This value is 0.65 at room temperature for eutectic solder(63Sn/37Pb).

Thermal damage to solder joints are most often caused by the followings:

- Global CTE (Coefficient of Thermal Expansion) mismatch between the package and board induces stresses. The package and board can also have temperature gradients through the thickness and at surface areas
- Local CTE mismatch between solder attachment to the component and the PWB

Reducing the CTE mismatch of component and PWB reduces cycling damages. For leaded SM package, the CTE mismatch on solder joint was relieved by compliant lead. Even though grid CSPs are robust in manufacturing, rigidity of are one of reliability concern.

For thermal cycling environment, several features of CSPs had help its reliability. These include reduction in package size and therefore die size and package thicknesses. Both these will improve reliability partially reducing the inherent reliability concern on CSPs. For high reliability applications, especially package with high I/Os, such improvement might not be sufficient and other innovative technology development required in order to decrease the local and global CTE mismatch.

Innovative approaches had been developed aimed at absorbing CTE mismatch between the die and board within the package or externally through strain absorbing mechanisms, and therefore reducing stresses on the solder interconnects. These innovative approaches could introduce their own unique damage mechanisms since possibly the weakest link now has been transferred from solder to other areas of the attachment system.

One innovative approach use compliant TAB lead and elastomeric materials between die and substrate to reduce the package CTE mismatch. Since the TABs absorb the majority of stresses, this become the weakest link and possible failure site. This approach has widely shown to be effective for low I/O CSPs, but yet to be proven for higher I/O CSPs. The other innovative approach which is called "Floating Pad Design" has potential for absorbing the global CTE mismatch and therefore, theoretically, it could handle a large I/O package. Test results by manufacturer is promising, but they are yet to be verified by others. It is not know if such solder ball floating would weaken the mechanical strength.

Underfill Effects on Reliability

Underfill has been widely used to improve an order of magnitude solder joint reliability of area array flip chip die attachment both for use in internal package and on-board. Underfill absorbs the CTE mismatch and therefore reduces significantly stress to a more uniform distribution on solder joint. Because of additional processes requirement; however, undefilling is undesirable both from cost increase and manufacturing throughputs. Another drawback of underfill is inability to rework defective parts. Progresses have been made to reduce the negative impact of underfilling by shortening process time using a snap cure polymers and enable reworkability by the development of reworkable underfills.

So, if we assume that underfill improves reliability, then one thought might be that if everything else failed to improve reliability of CSP, underfilling might be the ultimate undesirable solution. This approach for CSP was used by Sony when its passport size camera was introduce in early 1997. Effect of underfill for a wide range of CSPs are yet to be test validated to determine if solder joint improvement can achieved by underfilling. This paper presents cycles-to-failure data for three package assemblies with and without underfills with different reliability effects.

CSP TEST MATRIX

The Consortium agreed to concentrate on the following aspects of CSP technology and environmental testing after numerous workshops, meetings, and weekly teleconferences.

Package I/O /PWB (printed Wiring Board) — Ten packages from 28 to 275 as listed in Table 1. Figure 2 shows schematic cross-section drawing of package internal construction. The TSOP was used as control. PWBs were FR-4 and BT (Bismaleimide Triazine) materials which were available in the resin copper coated form and high temperature FR-4. The boards were double sided, standard and microvia. Four types of surface finishes were considered. Organic solder preservative (OSP), hot air solder leveling (HASL), and immersion Au/Ni and silver; the majority were OSP finish.

Solder Paste/Volume — Three types of solder pastes were included: no-clean, water soluble (WS), and rosin mildly activated (RMA). Three stencil thicknesses were included: high, standard, and low. The two extreme thicknesses were 4 and 7 mils with different stencil aperture design depending on the pad size. The standard which was used for the majority of test vehicles was 6 mil thickness.

Package/Test Vehicle Feature — All packages were daisy chained and they had up to two internal chain patterns. Packages had different pitches, solder ball volumes and compositions, and daisy chain patterns. In most cases, these patterns were irregular and much time and effort was required for design. This was especially cumbersome for packages with higher I/Os and many daisy chain mazes were develop. Packages with underfill requirements were included both with and without underfill to better understand the reliability consequence of not using underfill. The test vehicle was 4.5 by 4.5 inches and divided into four independent regions. For single side assembly, most packages can be cut for failure analysis without affecting the daisy chains of other packages.

Single-/Double-Sided Assembly — PWBs were double sided (microvia and standard) and several boards with double sided packages were assembled. This allowed direct reliability comparison between the standard and microvia technologies, single- and double-sided processing issues, and single- versus double-sided solder joint reliability. In designing daisy chains, it became apparent that the standard PWB technology could not be used for routing the majority of packages.

Underfill — Several assemblies were underfilled even though it was known that they may not require underfilling in order to understand dependency of underfill effect on solder joint reliability with package type. One packages required underfill, the majority were underfilled and several were not underfilled in order to better understand the reliability consequence of not using underfill.

Table 1 CSP Package Configurations Matrix

Package ID	Package. Type	Package Size (mm)	Pad Size (mm)	Pitch (mm)	I/O Count	Package. Thickness (mm)	Ball Dia (mm)
B	Leadless-1	7 x 13.6	0.35 x 0.7	0.8	28	0.8	-
C	TAB CSP-2	7.43 x 5.80	0.4	0.75	40	0.885	0.3
D	TSOP44	18.61 x 10.36	0.27 x 0.5	0.8	44	1.13	n/a
E	Leadless-2	7 x 12.3	0.30 x 0.75	0.5	46	0.8	n/a
F	TAB CSP-1	7.87 x 5.76	0.4	0.75	46	0.91	0.3
G	Chip on Flex-1 (COF-1)	0.3" x 0.3"	.010 in.	.020 in.	99	1.75	0.3
J	Wire Bond on Flex-1	12.1 x 12.1	0.375	0.8	144	1.4	0.5
K	Wire Bond on Flex-2	12 x 12	0.25	0.5	176	0.5	0.3
M	Chip on Flex-2 (COF-2)	0.5 x 0.5	.010 in.	.020 in.	206	1.75	0.3
N	Ceramic CSP	15 x 15	0.4	0.8	265	0.8	0.5
O	Wafer Level	0.413 x 0.413	.010 in.	.020 in.	275	-	0.3

• All measurements are in mm unless otherwise specified

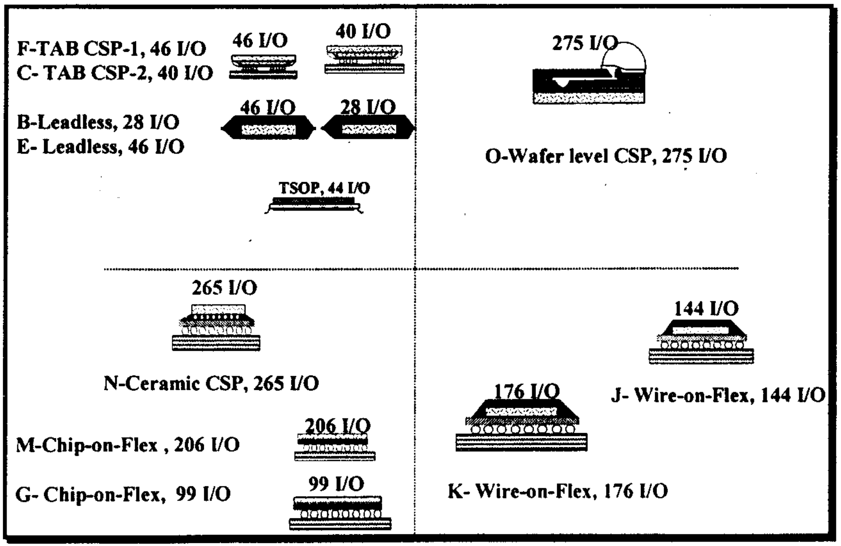

F-TAB CSP-1, 46 I/O
C- TAB CSP-2, 40 I/O
46 I/O
40 I/O
B-Leadless, 28 I/O
E- Leadless, 46 I/O
46 I/O
28 I/O
TSOP, 44 I/O
275 I/O
O-Wafer level CSP, 275 I/O
265 I/O
N-Ceramic CSP, 265 I/O
144 I/O
176 I/O
J- Wire-on-Flex, 144 I/O
M-Chip-on-Flex , 206 I/O
206 I/O
G- Chip-on-Flex, 99 I/O
99 I/O
K- Wire-on-Flex, 176 I/O

Figure 2 Schematic drawing of chip scale packages for the TV-1 test vehicle

Environmental testing — To link the data to those generated for the Ball Grid Array Consortium test, two conditions of –30° to 100°C (cycle A) and –55° to 125°C (Cycle B) were included. Two additional cycles were also investigated. Thermal cycling in the range of 0° to 100°C was performed to meet the needs of the commercial team members.

Hence, four different thermal cycle profiles were used. These were:

- Cycle A: The cycle A condition ranged from –30° to 100°C and had an increase/decrease heating rate of 2° to 5°C/min and dwell of about 20 minutes at the high temperature to assure near complete creep of the solder. The duration of each cycle was 82 minutes.
- Cycle B: The cycle B condition ranged from –55° to 125°C, with a very high heating/cooling rate. This cycle represent near thermal shock since it utilized a three region chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear with dwells at the extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.
- Cycle C: The cycle C condition ranged from –55° to 100°C with a short time duration at low temperature. The heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes.. The duration of each cycle was 90 minutes.
- Cycle D: The cycle D condition ranged from 0° to 100 °C with a 2-5°C/min heating/cooling rate. The Dwell at the extreme temperatures was at least 10 minutes, the cycle duration was 73 minutes.

Monitoring — The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life.

ENVIRONMENTAL TEST RESULTS

A large number of assemblies have already failed, and their cycles to failure have been documented. Out of these, cycles to failure data for three packages under four thermal cycling conditions are reviewed. Results for two chip on flex assemblies and leadless assemblies on single and double sided test vehicles are also presented. Results for other failed and survived assemblies are being gathered and analyzed and will be presented in future.

Cycles-to-Failures Under Four Conditions

Figure 3 compares cycles to failure test results for the M package with 206 I/Os under four thermal cycling conditions. The trends are as expected, i.e., as the thermal cycling temperature ranges increase, the cycles to failure decrease. Note that assemblies failed between 3 to 34 cycles under a near thermal shock in the range of -55 to 125 °C (B condition). Cycles to failure was 152 cycles under a typical commercial thermal cycling conditions in the ranges of 0 to 100°C. Results for -55/100°C and -30/100°C were between the two extreme cycling conditions as expected.

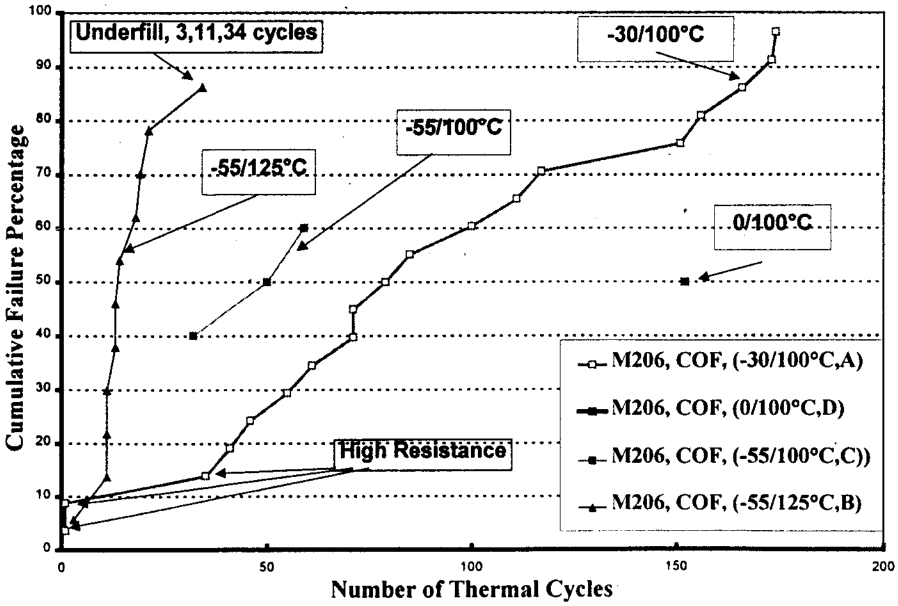


Figure 3 Cumulative Failure Distribution for Flex on Chip Assemblies with 206 I/Os Under Four Thermal Cycle Conditions

Cycles-to-failure for Assemblies with Underfill

Cycles-to-failure test results for several assemblies for different packages were analyzed to determine their failure with and without underfills. Representative examples for three categories relative to underfill impact on reliability are presented below.

Improvement by underfilling

Cycles-to-failure data for package B, leadless, 28 I/O with no underfill under A (-30 to 100°C) and B (-55 to 125°C) thermal cycling conditions are shown in Figure 4. As expected, cycles-to-failure increased as temperature cycling range decreased. Cycles-to-failure for B condition ranged from 372 to 546 with $N_{50\%}$ of 441 (cycles to 50% of test population).. For A condition, it ranged from 641 to 1007 cycles with $N_{50\%}$ of 763 cycles.

Results for 3 assemblies with underfill also shown in Figure 4. Underfilled assemblies showed only one failure at 1374 cycles under B condition to 1,500 cycles and no failure under A condition to 2,000 cycles. These limited test results clearly indicate significant improvement that can be achieved by underfilling for this category of peripheral leadless package.

Minimal impact by underfilling

Cycles-to-failure for package G, chip-o-flex, with 99 and package M with 206 I/Os with and without underfill B condition are shown in Figure 5. Cycles-to-failure were higher for package with lower I/O, but both assemblies showed extremely low failure cycles (,100 cycles). Three data points for assemblies with underfill are also shown. This limited data indicates that improvement due to underfilling for both package I/Os are almost insignificant.

Degradation by underfilling

Cycles-to-failure data points for package F, TAB CSP-1, with 46 I/Os under A and B thermal cycle conditions are summarized in Table 2. Under both conditions, assemblies with underfill showed much lower cycles to failure. For A condition to 2,000 cycles, there were no failure of assemblies without underfill, whereas the three assemblies with underfill failed. Note that this package decouples the effects of die CTE mismatch by adding a stress dampening elastomeric materials layer and using flexible TAB leads.

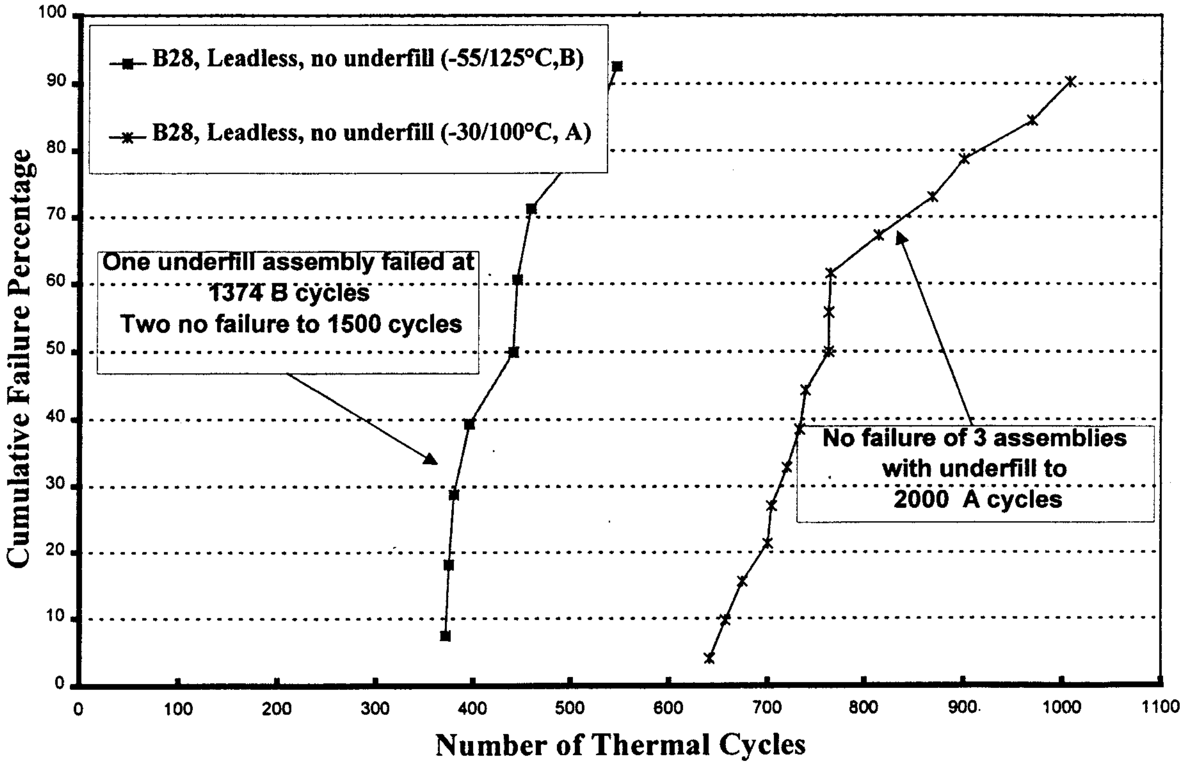


Figure 4 Cycles-to-failure for a 28 I/O leadless package without and with underfill

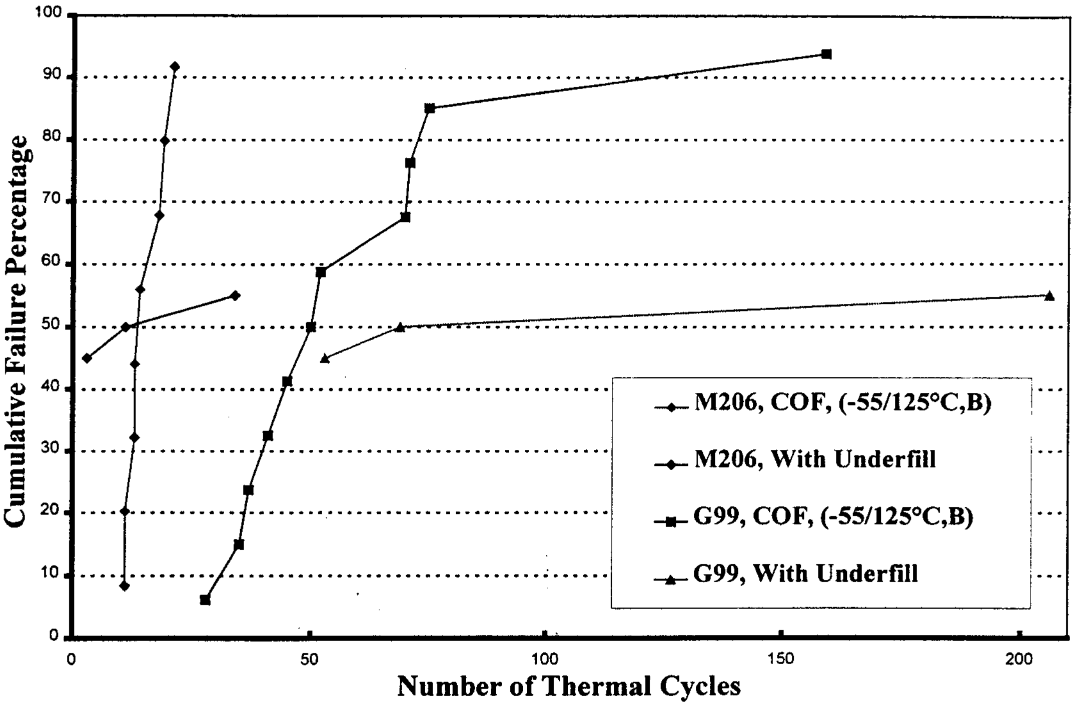


Figure 5 Cycles-to-failure for chip-on-flex assemblies with and without underfill

Table 2 Assemblies with and without underfill comparison

Package & thermal cycle condition	No Underfill Number and cycles to failure	With Underfill Number and cycles to failure
Package F, TAB CSP, -55°C to 125°C, B, 1,500 Cycles	3 out of 10 failure at 709, 896, and 1,380 cycles	3 out of 3 failures at 32 (?), 142, 710 cycles
Package F, TAB CSP-1, -30°C to 100°C, A, 2,000 cycles	No failure (15 assemblies)	3 out of 3 failure at 996, 1385, and 1727 cycles

CONCLUSIONS

- Cycles to failure for the same assembly under four different environments were different, but the trends were as expected. This means, as temperature cycling ranges increased, cycles to failure decreased.
- Underfill effects on cycles-to-failure may be positive, neutral, or negative depending on package types. It improved reliability of leadless package, was neutral for chip-on-flex, and had negative effects on the TAB CSP reliability.

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